Application Report

SNLA016B–May 2004–Revised May 2004

AN-643 EMI/RFI Board Design

ABSTRACT

The control and minimization of Electro-Magnetic Interference (EMI) is a technology that is, out of necessity, growing rapidly. EMI will be defined shortly but, for now, you might be more familiar with the terms Radio Noise, Electrical Noise, or Radio Frequency Interference (RFI). The technology's explorations include a wide frequency spectrum, from dc to 40 GHz. It also deals with susceptibility to EMI as well as the emissions of EMI by equipment or components. Emission corresponds to that potential EMI which comes out of a piece of equipment or component. Susceptibility, on the other hand, is that which couples from the outside to the inside.

Contents

1 INTRODUCTION 3
2 DESCRIPTION OF NOISE 3
2.1 ElectroMagnetic Interference 3
2.2 ElectroMagnetic Compatibility 4
2.3 Inter-System EMI 4
2.4 Coupling Paths 5
2.5 Conducted Interference 5
2.6 Radiated Interference 6
3 NOISE SOURCES 7
4 Cables and Connectors 7
5 Components 8
6 Power Supply Noise 8
7 High-Speed CMOS Logic Switching 11
8 Signal Crosstalk 12
9 Signal Interconnects 13
10 Ground Bounce 13
11 NOISE SUPPRESSION TECHNIQUES 14
12 Intra-System EMI-Control Techniques 15
12.1 Shielding 15
12.2 Filtering 16
12.3 Wiring 16
12.4 Inter-System EMI Control Techniques 18
13 DESIGN GUIDELINES 19
14 Logic Selection 19
15 Component Layout 20
16 Power Supply Bussing 21
17 Decoupling 23
18 Proper Signal Trace Layout 24
19 Ground Bounce 25
20 Components 26
21 Cables and Connectors 26
22 Special Considerations with Development Tools 27
23 NOISE MEASUREMENT 28
24 Environment 28
25 Instrumentation 29

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26 Cost 29
27 SUMMARY 30
28 REFERENCES 30

List of Figures

1 ElectroMagnetic Interference Situation 4
2 Intra-System EMI Manifestations 4
3 Simple Circuit Consisting of a Signal Source, V_S, and a Load, R_L 5
4 Differential-Mode Interference 5
5 Common-Mode Interference 6
6 Field-to-Cable Coupling 6
7 Cable-to-Cable Coupling 7
8 Common-Mode Impedance Coupling 7
9 Cables and Connectors 8
10 Diode Recovery Periods and Spikes 8
11 9
12 Switching Transients 9
13 Switching Transients When the Load Capacitance, C_L, is 15 pF 9
14 Switching Transients When the Load Capacitance, C_L, is 50 pF 10
15 Switching Transients When the Load Capacitance, C_L, is 100 pF 10
16 I_{CC} Current for a NAND Gate 10
17 Top Trace Shows Noise Induced on the High Logic Level Signal and the Bottom Trace Shows Noise Induced on the Low Logic Level Signal 11
18 Illustrates How Noise Affects a 74HC74's Clock Input 12
19 Crosstalk 12
20 Ground Bounce 14
21 Intra-System EMI Manifestations 15
22 Filtering 16
23 Board Layout 21
24 22
25 23
26 24
27 Series Termination 24
28 Parallel Termination 25
29 AC Parallel Termination 25
30 Thevenin Termination 25
31 Connectors 26
32 Alternating Signal Returns Minimizes Radiation 26
33 Single Signal Return Maximizes Radiation 27

List of Tables

1 Logic Family Comparisions 11
2 16
3 Electromagnetic Interference Coupling Paths 18
4 22

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1 INTRODUCTION

The control and minimization of Electro-Magnetic Interference (EMI) is a technology that is, out of necessity, growing rapidly. EMI will be defined shortly but, for now, you might be more familiar with the terms Radio Noise, Electrical Noise, or Radio Frequency Interference (RFI). The technology's explorations include a wide frequency spectrum, from dc to 40 GHz. It also deals with susceptibility to EMI as well as the emissions of EMI by equipment or components. Emission corresponds to that potential EMI which comes out of a piece of equipment or component. Susceptibility, on the other hand, is that which couples from the outside to the inside.

In HPC designs to date, we have looked at noise situations ranging from 2 MHz to 102 MHz. EMI, in some cases, can affect radio reception, TV reception, accuracy of navigation equipment, etc. In severe cases, EMI might even affect medical equipment, radar equipment, and automotive systems.

This Application Note will define ElectroMagnetic Interference and describe how it relates to the performance of a system. We will look at examples of Inter-system noise and Intra-system noise and present techniques that can be used to ensure ElectroMagnetic Compatibility throughout a system and between systems.

We will investigate and study the sources of noise between systems through wire-harness and backplane cables and connectors. Active circuit components can be contributors of noise and be susceptible to it. The fast switching times of CMOS devices fabricated in today's technology can cause incredible noise in a system. This noise typically is made up of crosstalk, power supply spiking, transient noise, and ground bounce.

The minimization and suppression of EMI can be obtained by utilizing proper control techniques. Intra-system noise, noise within a single module, sometimes can be controlled with methods such as filtering, shielding, careful selection of components, and following good wiring and grounding procedures. Controlling noise between systems, Inter-system noise, uses subtler techniques such as frequency management and time management, etc.

Appropriate time and resources should be spent during the design of a system or systems to insure that no problems will be encountered due to effects of EMI. Design guidelines will be presented that can be used to increase ElectroMagnetic Compatibility between systems by reducing the effects of noise between them. Above all, don't forget that the development tools used are also systems and are important to consider in your planning.

A brief look will be taken at the environment and tools required for different levels of noise testing. Relative risk-costs between preparing for EMC or excluding EMI concerns from the project will be listed.

2 DESCRIPTION OF NOISE

2.1 *ElectroMagnetic Interference*

EMI is a form of electrical-noise pollution. Think of the time when an electric drill or some other power tool jammed a nearby radio with buzzing or crackling noises. Sometimes it got so bad that it prevented you from listening to the radio while the tool was in use. Or the ignition of an automobile idling outside your house caused interference to your TV picture making lines across the screen or even losing sync altogether making the picture flip. These examples are quite annoying but not catastrophic.

More serious, how about a sudden loss in telephone communication caused by electrical interference or noise while you are negotiating an important business deal? Now EMI can be economically damaging.

The results of EMI incidences can be even farther reaching than these examples. Aircraft navigation errors resulting from EMI or interruption of air traffic controller service and maybe even computer memory loss due to noise could cause two aircraft to collide resulting in the loss of lives and property.

These were just a few examples to help you identify the results of EMI in a familiar context. To help understand an ElectroMagnetic Interference situation, the problem can be divided into three categories. They are the source, the victim, and the coupling path. Secondary categories involve the coupling path itself. It the source and victim are separated by space with no hard wire connection, then the coupling path is a radiated path and we are dealing with radiated noise. If the source and victim are connected together through wires, cables, or connectors, then the coupling path is a conducted path and we are dealing with conducted noise. Incidentally, both types of noise can exist at the same time.

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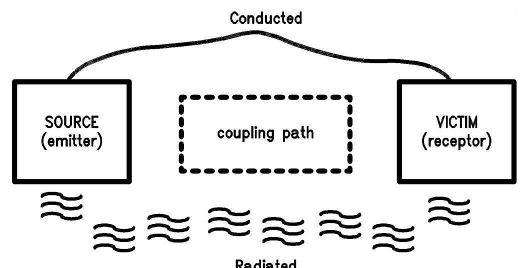

Figure 1. ElectroMagnetic Interference Situation

2.2 ElectroMagnetic Compatibility

If you think about the examples given, one can understand that EMI or electrical noise is of national concern. The Government and certain industry bodies have issued specifications with which all electrical, electromechanical, and electronic equipment must comply. These specifications and limitations are an attempt to ensure that proper EMC techniques are followed by manufactures during the design and fabrication of their products. When these techniques are properly applied, the product can then operate and perform with other equipment in a common environment such that no degradation of performance exists due to internally or externally conducted or radiated electromagnetic emissions. This is defined as ElectroMagnetic Compatibility or EMC.

2.3 Inter-System EMI

For the purpose of this Application Note, when the source of noise is a module, board, or system and the victim is a different and separate module, board, or system under the control of a different user, that is considered to be an inter-system interference situation. Examples of inter-system interference situations could be a Personal Computer interfereing with the operation of a TV or an anti-lock brake module in a car causing interference in the radio. This type of interference is more difficult to contain because, as mentioned earlier, the systems are generally not under the control of a single user. However, design methods and control techniques used to contain the intra-system form of EMI, which are almost always under the control of a single user, will inherently help reduce the inter-system noise.

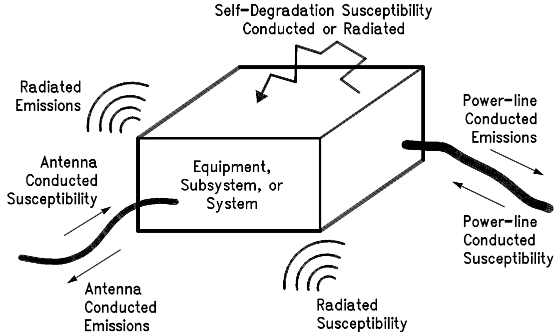

Figure 2. Intra-System EMI Manifestations

This Application Note will address problems and solutions in the area of intra-system noise. Intra-system interference situations are when the sources, victims, and coupling paths are entirely within one system or module or PC board. Systems may provide emissions that are conducted out power lines or be susceptible to emissions conducted in through them. Systems may radiate emissions through space as well as be susceptible to radiated noise. Noise conducted out antenna leads turns into radiated noise. By the same token, radiated noise picked up by the antenna is turned into conducted noise within the system. A perfect example is ground loops on a printed circuit board. These loops make excellent antennas. The system itself is capable of degrading performance due to its own internal generation of conducted and radiated noise and its susceptibility to it.

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Some results of EMI within a system: Noise on power line causing false triggering of logic circuits, rapidly changing signals causing “glitches” on adjacent steady state signal lines (crosstalk) causing erratic operation, mutiple simultaneously switching logic outputs propagating ground bounce noise throughout system, etc.

2.4 Coupling Paths

The modes of coupling an emitter source to a receptor victim can become very complicated. Remember, each EMI situation can be classified into two categories of coupling, conducted and radiated. Coupling can also result from a combination of paths. Noise can be conducted from an emitter to a point of radiation at the source antenna, then picked up at the receptor antenna by induction, and re-conducted to the victim. A further complication that multiple coupling paths presents is that it makes it difficult to determine if eliminating a suspected path has actually done any good. If two or more paths contribute equally to the problem, eliminating only one path may provide little apparent improvement.

2.5 Conducted Interference

In order to discuss the various ways in which EMI can couple from one system to another, it is necessary to define a few terms. When dealing with conducted interference, there are two varieties that we are concerned with. The first variety is differential-mode interference. That is an interference signal that appears between the input terminals of a circuit. The other variety of conducted interference is called common-mode interference. A common-mode interference signal appears between each input terminal and a third point; that third point is called the common-mode reference. That reference may be the equipment chassis, an earth ground, or some other point.

Let's look at each type of interference individually. In Figure 3 we show a simple circuit consisting of a signal source, V_S, and a load, R_L. In Figure 4 we show what happens when differential-mode interference is introduced into the circuit by an outside source. As is shown, an interference voltage, V_D, appears between the two input terminals, and an interference current, I_D, flows in the circuit. The result is noise at the load. If, for instance, the load is a logic gate in a computer, and the amplitude of V_D is sufficiently high, it is possible for the gate to incorrectly change states.

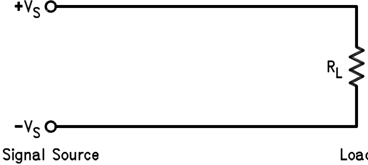

Figure 3. Simple Circuit Consisting of a Signal Source, V_S, and a Load, R_L

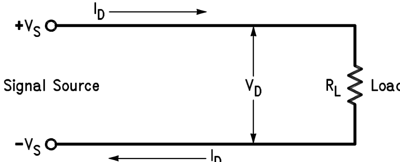

Figure 4. Differential-Mode Interference

Figure 5 shows what happens when a ground loop is added to our circuit. Ground loops, which are undesirable current paths through a grounded body (such as a chassis), are usually caused by poor design or by the failure of some component. In the presence of an interference source, common-mode currents, I_C, and a common-mode voltage, V_C, can develop, with the ground loop acting as the common-mode reference. The common-mode current flows on both input lines, and has the same instantaneous polarity and direction (the current and voltage are in phase), and returns through the common-mode reference. The common-mode voltage between each input and the common-mode reference is identical.

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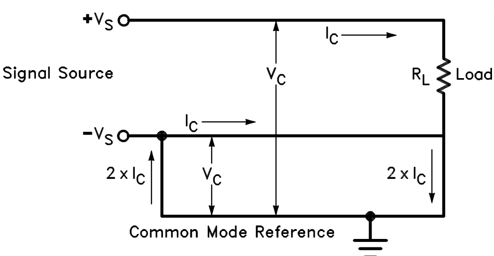

Figure 5. Common-Mode Interference

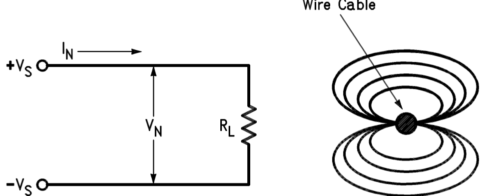

Figure 6. Field-to-Cable Coupling

2.6 Radiated Interference

Radiated coupling itself can take place in one of several ways. Some of those include field-to-cable coupling, cable-to-cable coupling, and common-mode impedance coupling. Let's look at those types of coupling one at a time.

The principle behind field-to-cable coupling is the same as that behind the receiving antenna. That is, when a conductor is placed in a time-varying electromagnetic field, a current is induced in that conductor. That is shown in Figure 6. In this figure, we see a signal source, V_S, driving a load, R_L. Nearby there is a current carrying wire (or other conductor). Surrounding the wire is an electromagnetic field induced by the current flowing in the wire. The circuit acts like a loop antenna in the presence of this field. As such, an interference current, I_N, and an interference voltage, V_N, are induced in the circuit. The magnitude of the induced interference signal is roughly proportional to the frequency of the incoming field, the size of the loop, and the total impedance of the loop.

Cable-to-cable coupling occurs when two wires or cables are run close to one another. Figure 7 shows how cable-to-cable coupling works. Figure 7*a* shows two lengths of cable (or other conductors) that are running side-by-side. Because any two conducting bodies have capacitance between them, called stray capacitance, a time-varying signal in one wire can couple via that capacitance into the other wire. That is referred to as capacitive coupling. This stray capacitance, as shown in Figure 7*c* makes the two cables behave as if there were a coupling capacitor between them. Another mechanism of cable-to-cable coupling is mutual inductance. Any wire carrying a time-varying current will develop a magnetic field around it. If a second conductor is placed near enough to that wire, that magnetic field will induce a similar current in the second conductor. That type of coupling is called inductive coupling. Mutual inductance, as shown in Figure 7*b*, makes the cables behave as if a poorly wound transformer were connected between them. In cable-to-cable coupling, either or both of those mechanisms may be responsible for the existance of an interference condition. Though there is no physical connection between the two cables, the properties we have just described make it possible for the signal on one cable to be coupled to the other.

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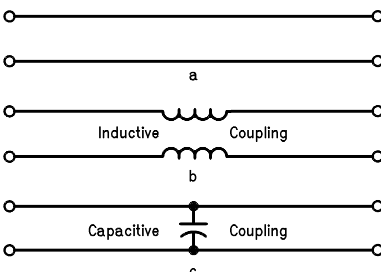

Figure 7. Cable-to-Cable Coupling

Either or both of the above-mentioned properties cause the cables to be electromagnetically coupled such that a time-varying signal present on one will cause a portion of that signal to appear on the other. The “efficiency” of the coupling increases with frequency and inversely with the distance between the two cables. One example of cable-to-cable coupling is telephone “crosstalk”, in which several phone conversations can be overheard at once. The term crosstalk is now commonly used to describe all types of cable-to-cable coupling.

Common-mode impedance coupling occurs when two circuits share a common bus or wire. In Figure 8 we show a circuit that is susceptible to that type of coupling. In that figure a TL092 op-amp and a 555 timer share a common return or ground. Since any conductor (including a printed circuit board trace) is not ideal, that ground will have a non-zero impedance, Z. Because of that, the current, I, from pin 1 of the 555 will cause a noise voltage, V_N, to develop; that voltage is equal to I × Z. That noise voltage will appear in series with the input to the op-amp. If that voltage is of sufficient amplitude, a noise condition will result.

While not all inclusive, these coupling paths account for, perhaps, 98% of all intra-system EMI situations.

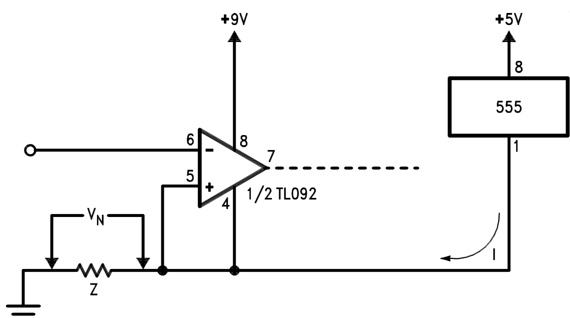

Figure 8. Common-Mode Impedance Coupling

3 NOISE SOURCES

In this Application Note, we will look at sources of EMI which involve components that may conduct or radiate electromagnetic energy. These sources, component emitters, are different from the equipment and subsystems we have been talking about. Component emitters are sources of EMI which emanate from a single element rather than a combination of components such as was previously described. Actually, these component emitters require energy and connecting wires from other sources to function. Therefore, they are not true sources of EMI, but are EMI Transducers. They convert electrical energy to electrical noise.

4 Cables and Connectors

The three main concerns regarding the EMI role of cables are conceptualized in Figure 9. They act as (1) radiated emission antennas, (2) radiated susceptibility antennas, and (3) cable-to-cable or crosstalk couplers. Usually, whatever is done to harden a cable against radiated emission will also work in reverse for controlling EMI radiated susceptibility. The reason for the word usually, is that when differential-mode radiated emission or susceptibility is the failure mode, twisting leads and shielding cables reduces EMI. If the failure mechanism is due to common-mode currents circulating in the cable, twisting leads has

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essentially no effect on the relationship between each conductor and the common-mode reference. Also cable shields may help or aggravate EMI depending upon the value of the transfer impedance of the cable shield. Transfer impedance is a figure of merit of the quality of cable shield performance defined as the ratio of coupled voltage to surface current in ohms/meter. A good cable shield will have a low transfer impedance. The effectiveness of the shield also depends on whether or not the shield is terminated and, if so, how it is terminated.

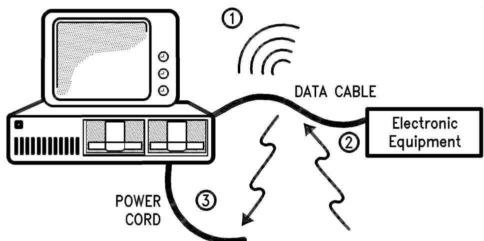

Figure 9. Cables and Connectors

Connectors usually are needed to terminate cables. When no cable shields or connector filters or absorbers are used, connectors play essentially no role in controlling EMI. The influence of connector types, however, can play a major role in the control of EMI above a few MHz. This applies especially when connectors must terminate a cable shield and/or contain lossy ferrites or filter-pins.

Connectors and cables should be viewed as a system to cost-effectively control EMI rather than to consider the role of each separately, even though each offers specific interference control opportunities.

5 Components

Under conditions of forward bias, a semiconductor stores a certain amount of charge in the depletion region. If the diode is then reverse-biased, it conducts heavily in the reverse direction until all of the stored charge has been removed as shown in Figure 10. The duration, amplitude, and configuration of the recovery-time pulse (also called switching time or period) is a function of the diode characteristics and circuit parameters. These current spikes generate a broad spectrum of conducted transient emissions. Diodes with mechanical imperfections may generate noise when physically agitated. Such diodes may not cause trouble if used in a vibration-free environment.

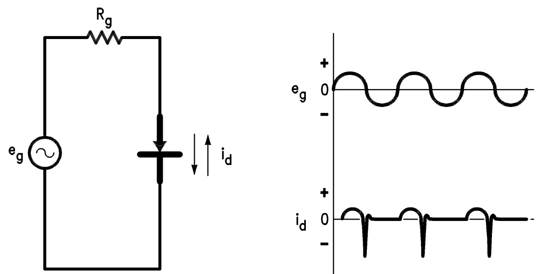

Figure 10. Diode Recovery Periods and Spikes

6 Power Supply Noise

Power-supply spiking is perhaps the most important contributor to system noise. When any element switches logic states, it generates a current spike that produces a voltage transient. It these transients become too large, they can cause logic errors because the supply voltage drop upsets internal logic, or because a supply spike on one circuit's output feeds an extraneous noise voltage into the next device's input.

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With CMOS logic in its quiescent state, essentially no current flows between V_{CC} and ground. But when an internal gate or an output buffer switches state, a momentary current flows from V_{CC} to ground. The switching transient caused by an unloaded output changing state typically equals 20 mA peak. Using the circuit shown in Figure 11, you can measure and display these switching transients under different load conditions.

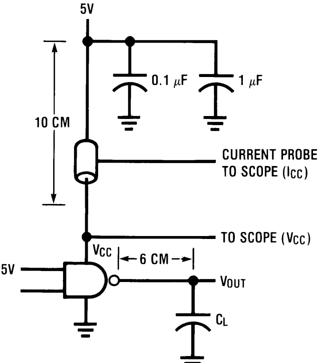

Figure 11.

Figure 12 shows the current and voltage spikes resulting from switching a single unloaded (C_L = 0 in Figure 11) NAND gate. These current spikes, seen at the switching edges of the signal on V_{IN}, increase when the output is loaded. Figure 13, Figure 14, and Figure 15 show the switching transients when the load capacitance, C_L, is 15 pF, 50 pF, and 100 pF, respectively. The large amount of ringing results from the test circuit's transmission line effects. This ringing occurs partly because the CMOS gate switches from a very high impedance to a very low one and back again. Even for medium-size loads, load capacitance current becomes a major current contributor.

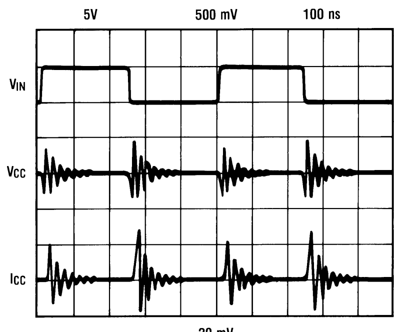

Figure 12. Switching Transients

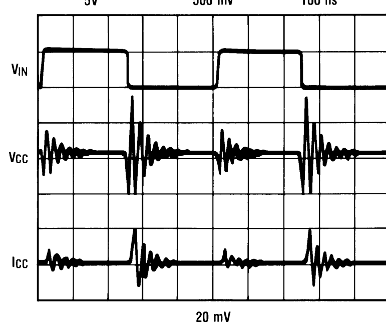

Figure 13. Switching Transients When the Load Capacitance, C_L, is 15 pF

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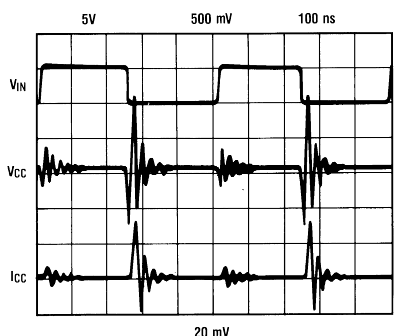

Figure 14. Switching Transients When the Load Capacitance, C_L, is 50 pF

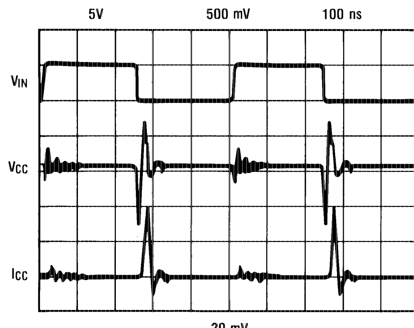

Figure 15. Switching Transients When the Load Capacitance, C_L, is 100 pF

Although internal logic generates current spikes when switching, the bulk of a spike's current comes from output circuit transitions. Figure 16 shows the I_{CC} current for a NAND gate, as shown in the test circuit, with one input switching and the other at ground resulting in no output transitions. Note the very small power-supply glitches provoked by the input-circuit transitions.

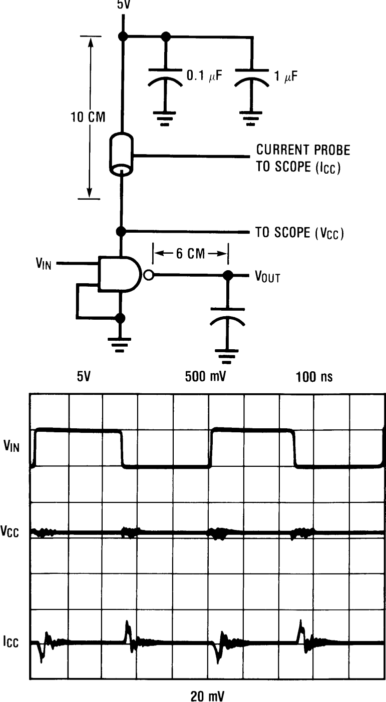

Figure 16. I_{CC} Current for a NAND Gate

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7 High-Speed CMOS Logic Switching

The magnitude of noise which can be tolerated in a system relates directly to the worst case noise immunity specified for the logic family. Noise immunity can be described as a device's ability to prevent noise on its input from being transferred to its output. It is the difference between the worst case output levels (V_{OH} and V_{OL}) of the driving circuit and the worst case input voltage requirements (V_{IH} and V_{IL}, respectively) of the receiving circuit.

Using Table 1 as a guide, it can be seen that for TTL (LS or ALS) devices the worst case noise immunity is typically 700 mV for the high logic level and 300 mV for the low logic level. For HCMOS devices the worst case noise immunity is typically 1.75V for high logic levels and 800 mV for low logic levels. AC high speed CMOS logic families have noise immunity of 1.75V for high logic levels and 1.25V for low logic levels. ACT CMOS logic families have noise immunity of 2.9V for high logic levels and 700 mV for low logic levels.

Table 1. Logic Family Comparisions

Characteristic	Symbol	LS/ALS TTL	HCMOS	AC	ACT
Input Voltage (Limits)	V_{IH} (Min)	2.0V	3.15V	3.15V	2.0V
	V_{IL} (Max)	0.8V	0.9V	1.35V	0.8V
Output Voltage (Limits)	V_{OH} (Min)	2.7V	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1
	V_{OL} (Max)	0.5V	0.1V	0.1V	0.1V

To illustrate noise margin and immunity, Figure 17 shows the output that results when you apply several types of simulated noise to a 74HC00's input. Typically, even 2V or more input noise produces little change in the output. The top trace shows noise induced on the high logic level signal and the bottom trace shows noise induced on the low logic level signal.

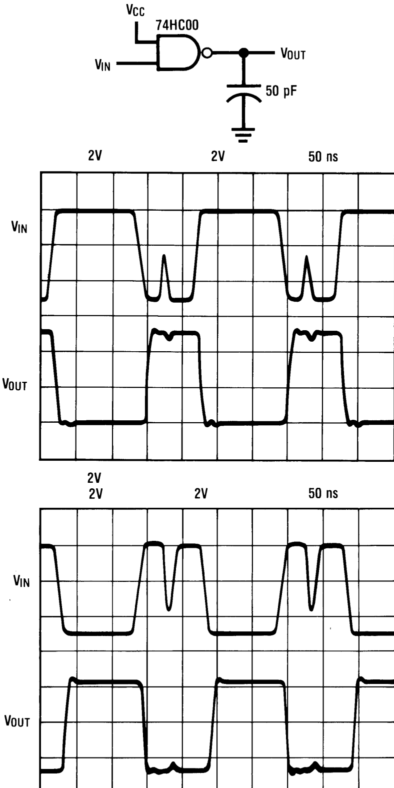

Figure 17. Top Trace Shows Noise Induced on the High Logic Level Signal and the Bottom Trace Shows Noise Induced on the Low Logic Level Signal

Figure 18 shows how noise affects a 74HC74's clock input. Again, no logic errors occur with 2V or more of noise on the clock input.

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When using high speed CMOS, even with its greater noise immunity, crosstalk, induced supply noise and noise transients become factors. Higher speeds allow the device to respond more quickly to externally induced noise transients and accentuate the parasitic interconnection inductances and capacitances that increase self-induced noise and crosstalk.

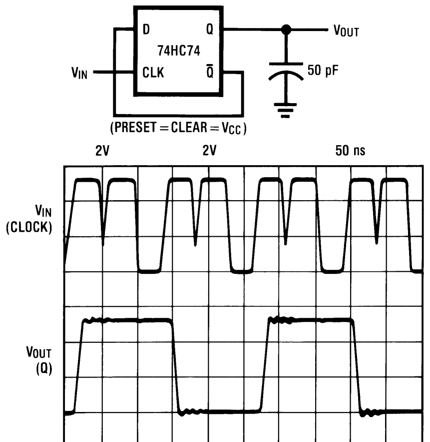

Figure 18. Illustrates How Noise Affects a 74HC74's Clock Input

8 Signal Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Our discussion on cable-to-cable coupling described crosstalk as appearing due to the distributed capacitive coupling and the distributed inductive coupling between two signal lines. When crosstalk is measured on an undriven sense line next to a driven line (both terminated at their characteristic impedances), the near end crosstalk and the far end crosstalk have quite distinct features, as shown in Figure 19. It should be noted that the near end component reduces to zero at the far end and vice versa. At any point in between, the crosstalk is a fractional sum of the near and far end crosstalk waveforms as shown in the figure. It also can be noted that the far end crosstalk can have either polarity whereas the near end crosstalk always has the same polarity as the signal causing it.

The amplitude of the noise generated on the undriven sense line is directly related to the edge rates of the signal on the driven line. The amplitude is also directly related to the proximity of the two lines. This is factored into the coupling constants K_{NE} and $K_{FE}$by terms that include the distributed capacitance per unit length, the distributed inductance per unit length, and the length of the line. The lead-to-lead capacitance and mutual inductance thus created causes “noise” voltages to appear when adjacent signal paths switch.

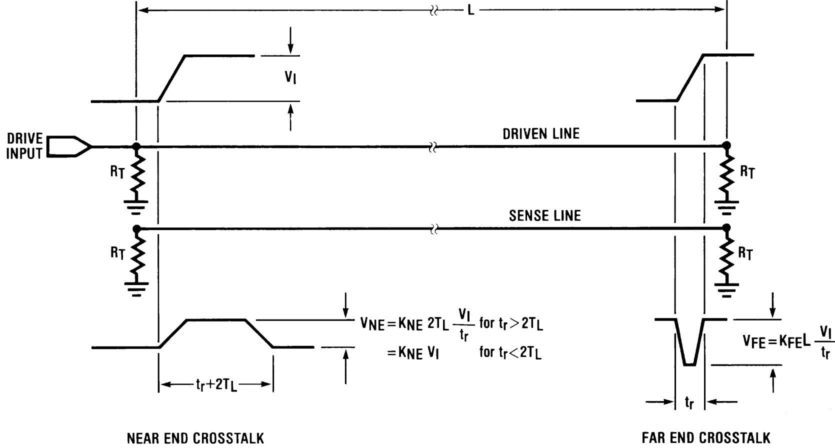

Figure 19. Crosstalk

Several useful observations that apply to a general case can then be made:

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- The crosstalk always scales with the signal amplitude V_I.
- Absolute crosstalk amplitude is proportional to slew rate V_I/t_r, not just $1/t_r$.
- Far end crosstalk width is always t_r.
- For $t_r < 2\ T_L$, where t_r is the transition time of the signal on the driven line and T_L is the propagation or bus delay down the line, the near end crosstalk amplitude V_{NE} expressed as a fraction of signal amplitude V_I is K_{NE} which is a function of physical layout only.
- The higher the value of "t_r"(slower transition times) the lower the percentage of crosstalk (relative to signal amplitude).

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than about three times the propagation delay of the line. Significant transmission line properties may be exhibited, for example, where devices having edge rates of 3 ns are used to drive traces of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

9 Signal Interconnects

Of the many properties of transmission lines, two are of major interest to the system designer: Z_{oe}, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_o and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z_{oe} and t_{pde} can be calculated with:

$$Z_{oe} = Z_o/(1 + C_t /C_i)^{**}0.5 \quad (1)$$

$$t_{pde} = t_{pd} * (1 + C_t/C_i)^{**}0.5 \quad (2)$$

where C_i = intrinsic line capacitance

C_t = additional capacitance due to gate loading.

These formulas indicate that the loading of lines *decreases* the effective impedance of the line and *increases* the propagation delay. As was mentioned earlier, lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

10 Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bondwires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced. One of these parasitic electrical characteristics is the inductance found in all leadframe materials.

Figure 20 shows a simple circuit model for a CMOS device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the output of the device.

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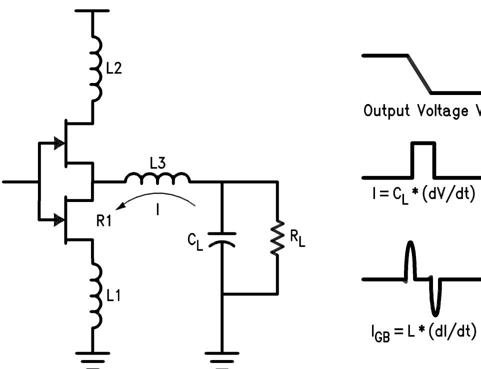

Figure 20. Ground Bounce

The three waveforms shown represent how ground bounce is generated. The top waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, and the inductors L1 and L3, and C_L, the load capacitance. In order to change the output from a HIGH to a LOW, current must flow to discharge the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = -C_L * (dV/dt)$]. This current, as it changes, causes a voltage to be generated across the inductances in the circuit. The formula for the voltage across an inductor is $V = L(dI/dt)$. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$V_{GB} = L1 * (dI/dt)$]. This induced voltage creates what is known as ground bounce.

Because the inductor is between the external system ground and the internal device ground, the induced voltage causes the internal ground to be at a different potential than the external ground. This shift in potential causes the device inputs and outputs to behave differently than expected because they are referenced to the internal device ground, while the devices which are either driving into the inputs or being driven by the outputs are referenced to the external system ground. External to the device, ground bounce causes input thresholds to shift and output levels to change.

Although this discussion is limited to ground bounce generated during HIGH-to-LOW transitions, it should be noted that the ground bounce is also generated during LOW-to-HIGH transitions. This ground bounce though, has a much smaller amplitude and therefore does not present the same concern.

There are many factors which affect the amplitude of the ground bounce. Included are:

- Number of outputs switching simultaneously: more outputs results in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60–70 pF, increases ground bounce. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load itself. Moving the load away from the output also reduces the ground bounce.
- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away due to effectively lower L1 and L3.
- Voltage: lowering V_{CC} reduces ground bounce.

Ground bounce produces several symptoms:

- Altered device states.
- Propagation delay degradation.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.

11 NOISE SUPPRESSION TECHNIQUES

EMI control techniques involve both hardware implementations and methods and procedures. They may also be divided into intra-system and inter-system EMI control. Our major concern in this Application Note is intra-system EMI control, however, an overview of each may be appropriate at this time.

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Figure 21 illustrates the basic elements of concern in an intra-system EMI problem. The test specimen may be a single box, an equipment, subsystem, or system (an ensemble of boxes with interconnecting cables). From a strictly near-sighted or selfish point-of-view, the only EMI concern would appear to be degradation of performance due to self jamming such as suggested at the top of the figure. While this might be the primary emphasis, the potential problems associated with either (1) susceptibility to outside conducted and/or radiated emissions or (2) tendency to pollute the outside world from its own undesired emissions, come under the primary classification of intra-system EMI. Corresponding EMI-control techniques, however, address themselves to both self-jamming and emission/susceptibility in accordance with applicable EMI specifications. The techniques that will be discussed include filtering, shielding, wiring, and grounding.

Inter-system EMI distinguishes itself by interference between two or more discrete and separate systems or platforms which are frequently under independent user control. Culprit emissions and/or susceptibility situations are divided into two classes: (1) antenna entry/exit and (2) back-door entry/exit. More than 95% of inter-system EMI problems involve the antenna entry/exit route of EMI. We can group inter-system EMI-control techniques by four fundamental categories: frequency management, time management, location management, and direction management.

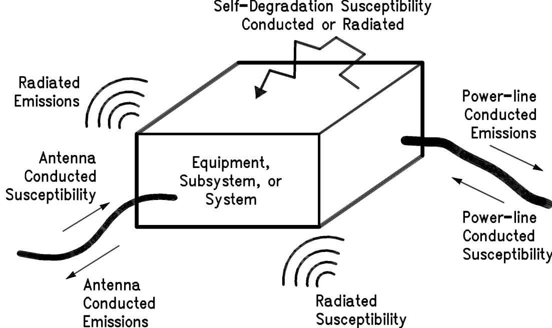

Figure 21. Intra-System EMI Manifestations

The first step in locating a solution is to identify the problem as either an inter-system or intra-system EMI situation. Generally, if the specimen has an antenna and the problem develops from what exits or enters the antenna from another specimen or ambient, then the problem is identified as an inter-system EMI one. Otherwise, it is an intra-system EMI situation which we will discuss now.

12 Intra-System EMI-Control Techniques

12.1 Shielding

Shielding is used to reduce the amount of electromagnetic radiation reaching a sensitive victim circuit. Shields are made of metal and work on the principle that electromagnetic fields are reflected and/or attenuated by a metal surface. Different types of shielding are needed for different types of fields. Thus, the type of metal used in the shield and the shield's construction must be considered carefully if the shield is to function properly. The ideal shield has no holes or voids, and, in order to accommodate cooling vents, buttons, lamps, and access panels, special meshes and “EMI-hardened” components are needed.

Once a printed-circuit board design has been optimized for minimal EMI, residual interference can be further reduced if the board is placed in a shielded enclosure. A box's shielding effectiveness in decibels depends on three main factors: its skin, the control of radiation leakage through the box's apertures or open areas (like cooling holes), and the use of filters or shields at entry or exit spots of cables.

A box skin is typically fabricated from sheet metal or metallized plastic. Normally sheet metal skin that is 1 mm thick is more than adequate; it has a shielding effectiveness of more than 100 dB throughout the high-frequency spectrum from 1 MHz to 20 GHz. Conductive coatings on plastic boxes are another matter. Table 2 shows that at 10 MHz the shielding effectiveness can be as low as 27 dB if a carbon composite is used, or it can run as high as 106 dB for zinc sprayed on plastic by an electric arc process. Plastic filled materials or composites having either conductive powder, flakes, or filament are also used in box shielding; they have an effectiveness similar to that of metallized plastics.

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Table 2.

Shielding Material	Surface Resistance [1] , Ohms/Square	Shielding Effectiveness, dB		
		At 10 MHz	At 100 MHz	At 1 GHz
Silver Acrylic	0.004	67	93	97
Paint				
Silver Epoxy	0.1	59	81	87
Paint				
Silver	0.05	57	82	89
Deposition				
Nickel	3.0	35	47	57
Composite				
Carbon	10.0	27	35	41
Composite				
Arc-Sprayed	0.002	106	92	98
Zinc				
Wire Screen	N.A.	86	66	48
(0.64 mm Grid)				

[1] Effectiveness of shielding materials with 25-μm thickness and for frequencies for which the largest dimension of the shielding plate is less than a quarter of a wavelength.

In many cases shielding effectiveness of at least 40 dB is required of plastic housings for microcontroller-based equipment to reduce printed-circuit board radiation to a level that meets FCC regulations in the United States or those of the VDE in Europe. Such skin shielding is easy to achieve. The problem is aperture leakage. The larger the aperture, the greater its radiation leakage because the shield's natural attenuation has been reduced. On the other hand, multiple small holes matching the same area as the single large aperture can attain the same amount of cooling with little or no loss of attenuation properties.

12.2 Filtering

Filters are used to eliminate conducted interference on cables and wires, and can be installed at either the source or the victim. Figure 22 shows an AC power-line filter. The values of the components are not critical; as a guide, the capacitors can be between 0.01 and 0.001 μF, and the inductors are nominally 6.3 μH. Capacitor C1 is designed to shunt any high-frequency differential-mode currents before they can enter the equipment to be protected. Capacitors C2 and C3 are included to shunt any common-mode currents to ground. The inductors, L1 and L2, are called common-mode chokes, and are placed in the circuit to impede any common-mode currents.

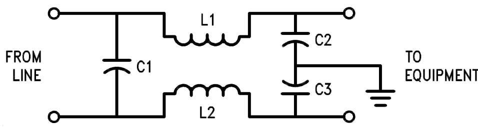

Figure 22. Filtering

12.3 Wiring

Now that the equipment in each box can be successfully designed to combat EMI emission and susceptibility separately, the boxes may be connected together to form a system. Here the input and output cables and, to a lesser extent, the power cable form an “antenna farm” that greatly threatens the overall electromagnetic compatibility of the system. Most field remedies for EMI problems focus on the coupling paths created by the wiring that interconnects systems. By this time most changes to the individual equipment circuits are out of the question.

Let us address five coupling paths that are encountered in typical systems comprised of two or more pieces of equipment connected by cables. These should adequately cover most EMI susceptibility problems. They are:

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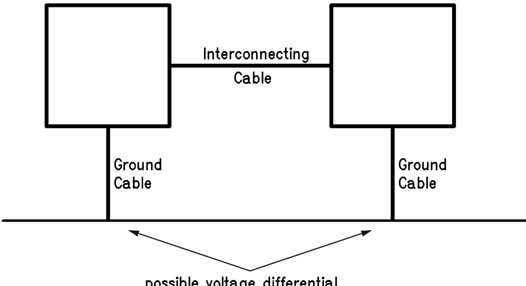
- *A common ground impedance coupling*—a conducting path in which a common impedance is shared between an undesired emission source and the receptor.
- *A common-mode, radiated field-to-cable coupling,* in which electromagnetic fields penetrate a loop formed by two pieces of equipment, a cable connecting them, and a ground plane.
- *A differential-mode, radiated field-to-cable coupling,* in which the electromagnetic fields penetrate a loop formed by two pieces of equipment and an interconnecting transmission line or cable.
- *A crosstalk coupling*, in which signals in one transmission line or cable are capacitively or inductively coupled into another transmission line.
- *A conductive path*through power lines feeding the equipment.

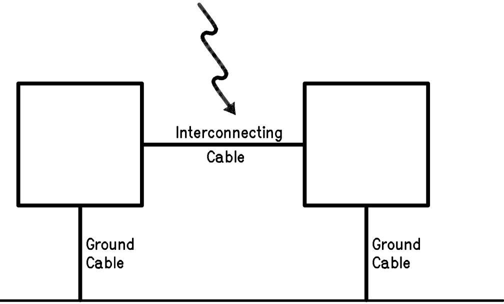
The first coupling path is formed when two pieces of equipment are connected to the same ground conductor at different points, an arrangement that normally produces a voltage difference between the two points. If possible, connecting both pieces of equipment to a single-point ground eliminates this voltage. Another remedy is to increase the impedance along a loop that includes the path between the ground connections of the two boxes. Examples include the isolation of printed-circuit boards from their cabinet or case, the use of a shielded isolation transformer in the signal path, or the insertion of an inductor between one or both boxes and the ground conductor. The use of balanced circuits, differential line drivers and receivers, and absorbing ferrite beads and rods on the interconnecting cable can further reduce currents produced by this undesirable coupling path.



Common Ground Impedance Coupling

A balanced circuit is configured so its two output signal leads are electrically symmetrical with respect to ground, as the signal increases on one output the signal on the other decreases. Differential line drivers produce a signal that is electrically symmetrical with respect to ground from a single-ended circuit in which only one lead is changing with respect to ground. Ferrite beads, threaded over electrical conductors, substantially attentuate electromagnetic interference by turning radio-frequency energy into heat, which is dissipated in them.

In the second coupling path, a radiated electromagnetic field is converted into a common-mode voltage in the ground plane loop containing the interconnect cable and both boxes. This voltage may be reduced if the loop area is trimmed.



Common-Mode, Radiated Field-to-Cable Coupling

The third coupling path produces a differential-mode voltage that appears across the input terminals of the EMI receptor. One way of controlling this is to cancel or block the pickup of differential-mode radiation. In a balanced transmission line, this is done by use of twisted-wire pairs and a shielded cable.

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As for crosstalk, the fourth coupling path—the reduction of capacitive coupling can be achieved by the implementation of at least one of these steps:

- Reducing the spacing between wire pairs in either or both of the transmission lines.
- Increasing the separation between the two transmission lines.
- Reducing the frequency of operation of the source, if possible.
- Adding a cable shield over either or both transmission lines.
- Twisting the source's or receptor's wire pairs.
- Twisting both wire pairs in opposite directions.

The fifth coupling path conductively produces both common-mode and differential-mode noise pollution on the power mains. Among several remedies that can suppress the EMI here are the filters and isolation transformers.

There are only about 50 common practical remedies that can be used in most EMI situations. Of these, about 10 suffice in 80 percent of the situations. Most engineers are aware of at least some of these remedies—for example, twisting wires to reduce radiation pickup.

In order to attack the EMI problem, one can make use of the information contained in Table 3. First, decide what coupling path has the worst EMI interference problem. From the 11 most common coupling paths listed at the top of the table, find the problem coupling path. Using the numbers found in that table entry, locate the recommended remedy or remedies from the 12 common EMI fixes identified at the bottom of the table. This procedure should be repeated until all significant coupling paths have been properly controlled and the design goal has been met.

12.4 Inter-System EMI Control Techniques

There are many EMI controls that may be carried out to enhance the chances of inter-system EMC. They can be grouped into four categories which we will discuss briefly. The following discussion is not intended to be complete but merely provide an overview of some EMI control techniques available to the intersystem designer and user.

Frequency management suggests both transmitter emission control and improvement of receptors against spurious responses. The object is to design and operationally maintain transmitters so that they occupy the least frequency spectrum possible in order to help control electromagnetic pollution. For example, this implies that long pulse rise and fall times should be used. Quite often one of the most convenient, economic and rapid solutions to an EMI problem in the field, is to change frequency of either the victim receiver or the culprit source.

In those applications where information is passed between systems, a possible time management technique could be utilized where the amount of information transferred is kept to a minimum. This should reduce the amount of time that the receptor is susceptible to any EMI. In communication protocols, for example, essential data could be transmitted in short bursts or control information could be encoded into fewer bits.

Location management refers to EMI control by the selection of location of the potential victim receptor with respect to all other emitters in the environment. In this regard, separation distance between transmitters and receivers is one of the most significant forms of control since interfering source emissions are reduced greatly with the distance between them. The relative position of potentially interfering transmitters to the victim receiver are also significant. If the emitting source and victim receiver are shielded by obstacles, the degree of interference would be substantially reduced.

Direction management refers to the technique of EMI control by gainfully using the direction and attitude of arrival of electromagnetic signals with respect to the potential victim's receiving antenna.

Table 3. Electromagnetic Interference Coupling Paths

Radiated Field to Interconnecting Cable	2, 7, 8, 9, 11	Radiated Field to Box	12, 13
(Common-Mode)			
Radiated Field to Interconnecting Cable	2, 5, 6	Box to Radiated Field	12, 13
(Differential-Mode)			
Interconnecting Cable to Radiated Field	1, 3, 9, 11	Box-to-Box Radiation	12, 13

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Table 3. Electromagnetic Interference Coupling Paths (continued)

(Common-Mode)			
Interconnecting Cable to Radiated Field	1, 3, 5, 6, 7	Box-to-Box Conduction	1, 2, 7, 8, 9
(Differential-Mode)			
Cable-to-Cable Crosstalk	1, 2, 3, 4, 5, 6, 10, 11	Power Mains to Box Conduction	4, 11
		Box to Power Mains Conduction	4

Electromagnetic Interference Fixes

1. **Insert Filter In Signal Source**
2. **Insert Filter in Signal Receptor**
3. **Insert Filter in Power Source**
4. **Insert Filter in Power Receptor**
5. **Twist Wire Pair**
6. **Shield Cable**
7. **Use Balanced Circuits**
8. **Install Differential Line Drivers and Receivers**
9. **Float Printed Circuit Board(s)**
10. **Separate Wire Pair**
11. **Use Ferrite Beads**
12. **Use a Multilayer Instead of a Single-Layer Printed Circuit Boards**

13 DESIGN GUIDELINES

The growth of concern over electromagnetic compatibility (EMC) in electronic systems continues to rise in the years since the FCC proclaimed that there shall be no more pollution of the electromagnetic spectrum. Still, designers have not yet fully come to grips with a major source and victim of electromagnetic interference—the printed circuit board. The most critical stage for addressing EMI is during the circuit board design. Numerous tales of woe can be recounted about the eleventh hour attempt at solving an EMI problem by retrofit because EMC was given no attention during design. This retrofit ultimately costs much more than design stage EMC, holds up production, and generally makes managers unhappy. With these facts in mind, let's address electromagnetic compatibility considerations in printed circuit board design.

14 Logic Selection

Logic selection can ultimately dictate how much attention must be given to EMC in the total circuit design. The first guideline should be: use the slowest speed logic that will do the job. Logic speed refers to transition times of output signals and gate responses to input signals. Many emissions and susceptibility problems can be minimized if a slow speed logic is used. For example, a square wave clock or signal pulse with a 3 ns rise time generates radio frequency (100 MHz and higher) energy that is gated about on the PC board. It also means that the logic can respond to comparable radio frequency energy if it gets onto the boards.

The type of logic to be used is normally an early design decision, so that control of edge speeds and, hence, emissions and susceptibility is practical early. Of course, other factors such as required system performance, speed, and timing considerations must enter into this decision. If possible, design the circuit with a slow speed logic. The use of slow speed logic, however, does not guarantee that EMC will exist when the circuit is built; so proper EMC techniques should still be implemented consistently during the remainder of the circuit design.

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15 Component Layout

Component layout is the second stage in PC board design. Schematics tell little or nothing about how systems will perform once the board is etched, stuffed, and powered. A circuit schematic is useful to the design engineer, but an experienced EMC engineer refers to the PC board when troubleshooting. By controlling the board layout in the design stage, the designer realizes two benefits: (1) a decrease in EMI problems when the circuit or system is sent for EMI or quality assurance testing; and (2) the number of EMI coupling paths is reduced, saving troubleshooting time and effort later on.

Some layout guidelines for arranging components according to logic speed, frequency, and function are shown in Figure 23. These guidelines are very general. A particular circuit is likely to require a combination and/or tradeoffs of the above arrangements. Isolation of the I/O from digital circuitry is important where emissions or susceptibility may be a problem. For the case of emissions, a frequently encountered coupling path involves a digital energy coupling through I/O circuitry and signal traces onto I/O cables and wires, where the latter subsequently radiate. When susceptibility is a problem, it is common for the EMI energy to couple from I/O circuits onto sensitive digital lines, even though the I/O lines may be “opto-coupled” or otherwise supposedly isolated. In both situations, the solution often lies in the proper electrical and physical isolation of analog and low speed digital lines from high speed circuits. When high speed signals are designed to leave the board, the reduction of EMI is usually performed via shielding of I/O cables and is not considered here.

Therefore, a major guideline in laying out boards is to isolate the I/O circuitry from the high speed logic. This method applied even if the logic is being clocked at “only” a few MHz. Often, the fundamental frequency is of marginal interest, with the harmonics generated from switching edges of the clock being the biggest emission culprits. Internal system input/output PCB circuity should be mounted as close to the edge connector as possible and capacitive filtering of these lines may be necessary to reduce EMI on the lines.

High speed logic components should be grouped together. Digital interface circuitry and I/O circuitry should be physically isolated from each other and routed on separate connectors, if possible as shown in Figure 23*d*.

- No High Frequency Signals to the Backplane

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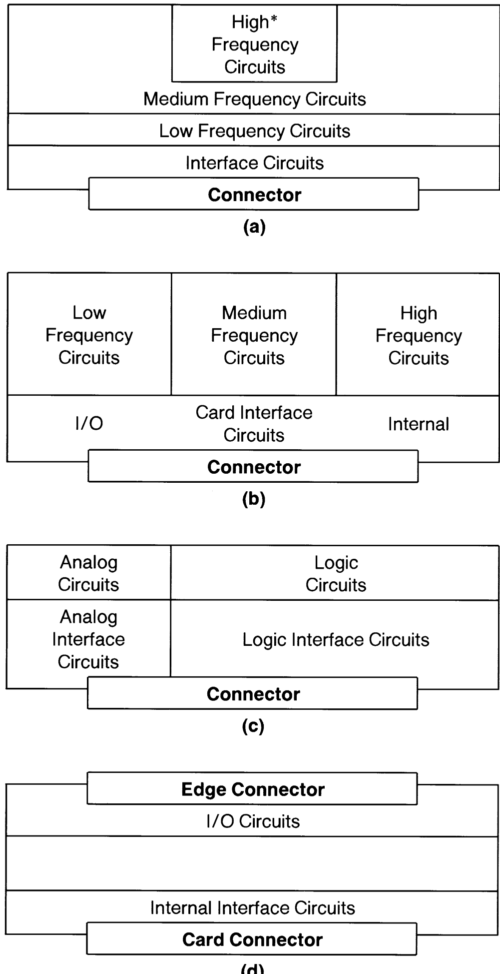

Figure 23. Board Layout

16 Power Supply Bussing

Power supply bussing is the next major concern in the design phase. Isolated digital and analog power supplies must be used when mixing analog and digital circuitry on a board. The design preferably should provide for separate power supply distribution for both the analog and digital circuitry. Single point common grounding of analog and digital power supplies should be performed at one point and one point only—usually at the motherboard power supply input for multi-card designs, or at the power supply input edge connector on a single card system. The fundamental feature of good power supply bussing, however, is low impedance and good decoupling over a large range of frequencies. A low impedance distribution system requires two design features: (1) proper power supply and return trace layout and (2) proper use of decoupling capacitors.

At high frequencies, PCB traces and the power supply busses (+V_{CC} and 0V) are viewed as transmission lines with associated characteristic impedance, Z_O, as modeled in Figure 24. The goal of the designer is to maximize the capacitance between the lines and minimize the self-inductance, thus creating a low Z_O. Table 4 shows the characteristic impedance of various two-trace configurations as a function of trace width, W, and trace separation, h.

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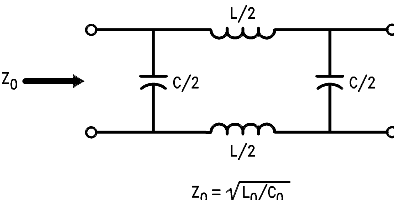
Table 4. [(1)]

W/h or D/W	#1 Z_{01} Parallel Strips*	#2 Z_{02} Strip Over Ground Plane*	#3 Z_{03} Strips Side by Side**
0.5	377	377	NA
0.6	281	281	NA
0.7	241	241	NA
0.8	211	211	NA
0.9	187	187	NA
1.0	169	169	0
1.1	153	153	25
1.2	140	140	34
1.5	112	112	53
1.7	99	99	62
2.0	84	84	73
2.5	67	67	87
3.0	56	56	98
3.5	48	48	107
4.0	42	42	114
5.0	34	34	127
6.0	28	28	137
7.0	24	24	146
8.0	21	21	153
9.0	19	19	160
10.0	17	17	166
12.0	14	14	176
15.0	11.2	11.2	188
20.0	8.4	8.4	204
25.0	6.7	6.7	217
30.0	5.6	5.6	227
40.0	4.2	4.2	243
50.0	3.4	3.4	255

(1) *Mylar dielectric assumed: DC = 5.0; D≫ nearby ground plane
**Paper base phenolic or glass epoxy assumed: DC = 4.7

$$Z01 = (377/\sqrt{DC}) \times (h/W), \text{ for } W > 3h \text{ and } h > 3t$$
$$Z02 = (377/\sqrt{DC}) \times (h/W), \text{ for } W > 3h$$
$$Z03 = (120/\sqrt{DC}) \text{ lne } (D/W + \sqrt{D/W^2 - 1}) \text{ for } W \gg t \quad (3)$$



where L_O and C_O are, respectively, the distributed inductance and capacitance per unit length of the line

Figure 24.

Any one of the three configurations may be viewed as a possible method of routing power supply (or signal) traces. The most important feature of Table 4 is the noticeable difference in impedance between the parallel strips and strip over ground plane compared with the side-by-side configurations.

As an example of the amount of voltage that can be generated across the impedance of a power bus, consider TTL logic which pulls a current of approximately 16 mA from a supply that has a 25Ω bus impedance (this assumes no decoupling present). The transient voltage is approximately dV = 0.016 × 25Ω = 400 mV, which is equal to the noise immunity level of the TTL logic. A 25Ω (or higher) impedance is not uncommon in many designs where the supply and return traces are routed on the same side of the board in a side-by-side fashion. In fact, it is not uncommon to find situations where the power supply and return traces are routed quite a distance from each other, thereby increasing the overall impedance of the distribution system. This is obviously a poor layout.

Power and ground planes offer the least overall impedance. The use of these planes leads the designer closer to a multi-layer board. At the very least, it is recommended that all open areas on the PC board be "landfilled" with a 0V reference plane so that ground impedance is minimized.

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Multi-layer boards offer a considerable reduction in power supply impedance, as well as other benefits. As shown in Table 4, the impedance of a multi-layer power/ground plane bus grows very small (on the order of an ohm or less), assuming a W/h ratio greater than 100. Multi-layer board designs also pay dividends in terms of greatly reduced EMI, and they provide close control of line impedances where impedance matching is important. In addition, shielding benefits can be realized. For high-density, high-speed logic applications, the use of a multi-layer board is almost mandatory. The problem with multi-layer boards is the increased cost of design and fabrication and increased difficulty in board repair.

17 Decoupling

High-speed CMOS has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with CMOS devices in system performance and EMC performance.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to a HIGH value. This power is necessary to charge the load capacitance or drive a line impedance.

For most power distribution networks, the typical impedance can be between 50 and 100Ω. This impedance appears in series with the load impedance and will cause a droop in the V_{CC} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example presented in Figure 25 used to help calculate the amount of decoupling necessary. This circuit utilizes an octal buffer driving a 100Ω bus from a point somewhere in the middle.

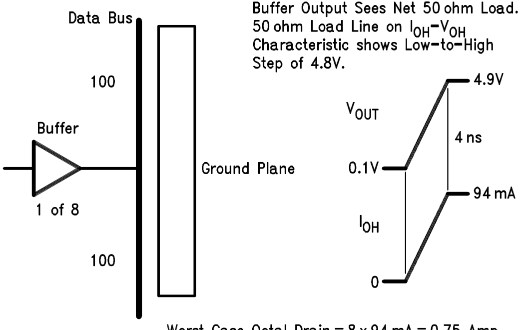

Figure 25.

Being in the middle of the bus, the driver will see two 100Ω loads in parallel, or an effective impedance of 50Ω. To switch the line from rail to rail, a drive of 94 mA is needed (4.8V/50Ω) and more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will be to lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current demands. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in Figure 26.

In this example, if the V_{CC} droop is to be kept below 0.1V and the edge rate equals 4 ns, we can calculate the value of the decoupling capacitor by use of the charge on a capacitor equation: Q = CV. The capacitor must supply the high demand current during the transition period and is represented by I = C (dV/dt). Rearranging this somewhat yields C = I (dt/dV).

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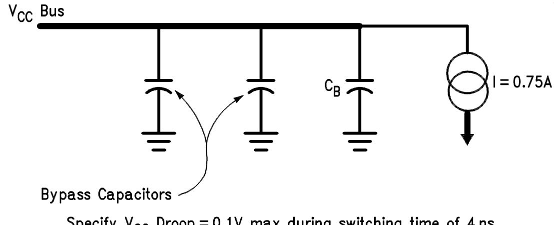

Q = CV charge on capacitor
I = C dV/dt
C = I dt/dV = 750 mA x 4 ns / 0.1V = 0.030 µF
Select C_B = 0.047 µF or greater

Figure 26.

Now, I = 750 mA assuming all 8 outputs switch simultaneously for worst case conditions, dt = switching period or 4 ns, and dV is the specified V_{CC} droop of 0.1V. This yields a calculated value of 0.030 µF for the decoupling capacitor. So, a selection of 0.047 µF or greater should be sufficient.

It is good practice to distribute decoupling capacitors evenly throughout the logic on the board, placing one capacitor for every package as close to the power and ground pins as possible. The parasitic induction in the capacitor leads can be greatly reduced or eliminated by the use of surface mount chip capacitors soldered directly onto the board at the appropriate locations. Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

18 Proper Signal Trace Layout

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

For those situations where lines must run parallel as in address and data buses, the effects of crosstalk can be minmized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing.

There are several termination schemes which may be used. They are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula:

$$V_W = V_{CC} * Z_{oe} / (Z_{oe} + R_S + Z_S) \tag{4}$$

source load

Figure 27. Series Termination

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance (Z_{oe}). The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

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Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground depending on which bus the resistor is connected to. While this feature is not desirable for driving CMOS inputs because the trip levels are typically $V_{CC}/2$, it can be useful for driving TTL inputs where level shifting is desirable in order to interface with CMOS devices.

Figure 28. Parallel Termination

AC parallel terminations work well for applications where the increase in bus delays caused by series terminations are undesirable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

Thevenin terminations are not generally recommended due to their power consumption.

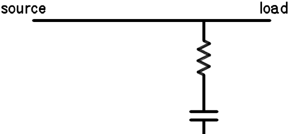

Figure 29. AC Parallel Termination

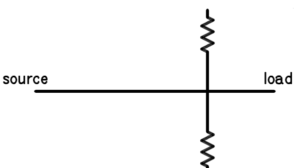

Figure 30. Thevenin Termination

Like parallel terminations, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally be independent of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that output lines with Thevenin terminations should not be left floating since this will cause the undriven input levels to float between V_{CC} and ground, increasing power consumption.

19 Ground Bounce

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

- First, use caution when driving asynchronous TTL-level inputs from CMOS octal outputs. Ground bounce glitches may cause spurious inputs that will alter the state of non-clocked logic.
- Second, use caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.
  - When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:
- Choose package outputs that are as close to the ground pin as possible to drive asynchronous TTL-level inputs.
- Use the lowest V_{CC} possible or separate the power supplies.

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- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

20 Components

The interference effect by rectifier diodes, typically found in power supply sections of PC boards, can be minmized by one or more of the following measures:

- Placing a bypass capacitor in parallel with each rectifier diode.
- Placing a resistor in series with each rectifier diode.
- Placing an R-F bypass capacitor to ground from one or both sides of each rectifier diode.
- Operating the rectifier diodes well below their rated current capability.

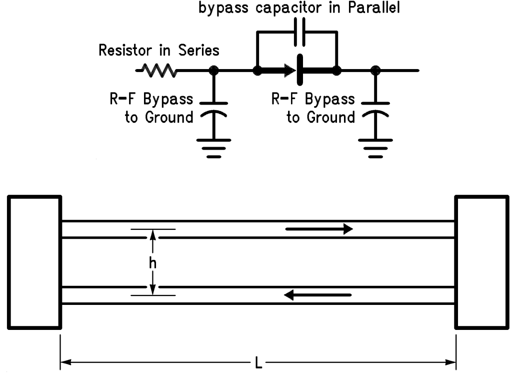

Figure 31. Connectors

21 Cables and Connectors

Several options are available to reduce EMI from a typical ribbon cable used to interconnect pieces of equipment. These include:

- Reduce spacing between conductors (h in the figure) by reducing the size of wires used and reducing the insulation thickness.
- Join alternate signal returns together at the connectors at each end of the cable.
- Twist parallel wire pairs in ribbon cables.
- Shield ribbon cable with metal foil cover (superior to braid).
- Replace discrete ribbon cable with stripline flexprint cable.

In the case of joining alternate signal returns, wire N is carryig the signal current, i_n, whereas its mates, N−1 and N+1 wires are each carrying one half of the return currents, i_{n-1} and i_{n+1}, respectively. Thus, radiation from pair N and N−1 is out of phase with radiation from pair N and N+1 and will tend to cancel. In practice, however, the net radiation is reduced by 20–30 dB with 30 dB being a good default value.

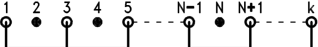

Figure 32. Alternating Signal Returns Minimizes Radiation

The opposite of this is to conserve signal returns by only using one, or two, wires to service N data lines in a ribbon cable. For data lines farther from the return line, the differential mode radiation becomes so great that this cable tends to maximize EMI radiation. Another disadvantage of this approach is poor impedance control in the resulting transmission line. This could result in distortion of pulses and cause reflections, especially for high-speed logic, and common return impedance noise in this single ground wire.

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(k−1)/2

(K−1)/2 − 1 (K−1)/2 + 1

Figure 33. Single Signal Return Maximizes Radiation

Ideally, connectors should have negligible resistance for obvious reasons other than EMI control. They should provide foolproof alignment to minimize the possibility of contact damage over time and use which would increase the resistance and be prone to vibration and shock. Adequate force to provide good mating between contacts which will insure low resistance and limit likelihood of damage. Connectors should mate with little friction to minimize the effects of continual disconnections and connections increasing the contact resistance with use as the contacts wear out. A contamination free design should be used to avoid corrosion and oxidation increasing resistance and susceptibility to shock and vibration causing intermittent contact.

22 Special Considerations with Development Tools

The following set of guidelines have been compiled from the experiences of the Development Systems Group and the Microcontroller Applications Group in Santa Clara. They should be considered *additional* techniques and guidelines to be followed concurrently with the standard ones already presented. Some are general and some may be specific to development systems use.

Ground bounce prevention and minimization techniques presented in this Application Note should be strictly adhered to when using '373 type transparent latches on the HPC's external address/data bus. Multiple simultaneously switching outputs could produce ground bounce significant enough to cause false latching. Observe good EMI planning by locating the latches as close to the HPC as possible. The use of multi-layer printed circuit boards with good ground planes and following appropriate layout techniques is also essential, especially if emulation will be done at frequencies above 10 MHz. With the foregoing discussions about “antenna farms”, radiated noise, and ideal connector characteristics, it becomes obvious that wire-wrap boards and the use of IC sockets is absolutely out of the question. The concern here is not so much EMI affecting the outside world but EMI strangling the operation of the module itself.

The inputs to the buffers in a '244 type octal buffer package are placed adjacent or side-by-side outputs of other buffers in the package. This configuration would tend to maximize the crosstalk or noise coupling from the inputs to the outputs. On the other hand, the buffer inputs in a '544 type package are on one side of the package and the outputs are on the other. The use of these package types in high speed designs can facilitate board layout to help reduce the effects of crosstalk.

Use extra heavy ground wires between emulator and target board. Rely on the ground returns in the emulator cable for reduction of differential-mode noise radiated from the cable but heavy-duty help is required for reducing power line impedance in the integrated development system.

Unused HPC inputs, most importantly NMI and RDY/$\overline{\text{HLD}}$, must be tied to V_{CC} directly or through a pull-up resistor. This not only tends to reduce power consumption, but will avoid noise problems triggering an unwanted action.

In order to reduce the effects of noise generated by high speed signal changes, a sort of Frequency Management technique might be applied. If possible, develop application hardware and software at a slower crystal operating frequency. If ringing, crosstalk, or other combinations of radiated and conducted noise problems exist, the result may be to move the problem from one point in the affected signal waveform to a different point. Thus, apparent “noise glitches” that caused a latch to erroneously trigger when the input data was still changing, may now come at a time when they are non-destructive such as at a point when the input data is now stable.

Some applications require driving the HPC clock input, CKI, with an external signal. The emulator tools are all clocked using a crystal network with the HPC so that the generation of the system timing is contained on the tool itself. Consequently, there is no connection between the emulator cable connector on the tool and the CKI pin at the HPC. However, when the emulator cable is now inserted into the target board, the target board's clock signal travelling along the cable couples noise onto adjacent signal lines causing symptoms pointing to an apparent failure of the emulator tool. The recommendation is to disable the clock drive to the CKI pin at the HPC pad on the target board whenever the emulator tool is

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connected. The emulator tools supply the system clock so there is no need for the clock on the target and signal crosstalk on the emulator cable can be greatly reduced with minimal implementation. If one insists that the emulator tool and the target be synchronous, then bring the clock signal from the target to the emulator tool external to the emulator cable via twisted wire pair or coax cable. Remove the clock drive connection to CKI at the target to prevent the signal from entering the cable. Finally, remove crystal components on emulator tool to prevent problems with the signal.

Connecting boards and modules together to make a totally unique system in which EMC was practiced is necessary to ensure little problem with the environment. But, connecting an emulator tool makes it an entirely new and unique system, both in physical and electrical properties. Treat the emulator tool as part of the system during the design phase and development phase.

23 NOISE MEASUREMENT

The basic purpose of FCC Part 15J is to minimize the jamming of commercial broadcasting systems by computer devices. Toward this end, the FCC has established test limits, for both conducted and radiated emissions, which must be met. These two tests together span the frequency range from 450 kHz to 1000 MHz. To accomplish FCC Part 15J testing requires the following equipment and associated support items:

- EMC Receivers or Spectrum Analyzers to cover the frequency range from 450 kHz to 1000 MHz.
- Dipole antennas (2) to cover the frequency range from 30 MHz to 1000 MHz.
- Masts or supports which will allow antenna elevation to be increased to at least 4 meters and also allow the polarization to be changed.
- Line impedance stabilization networks (LISN) built in accordance with CISPR requirements. These are 50Ω, 50 μH devices and are inserted between power mains and test item to permit making repeatable conducted EMI measurements.
- Power line filters.
- An appropriate test site.

24 Environment

The most controversial item on the test requirement list is the appropriate test site. The FCC required emission limits are comparable with the ambient RF level. These low limits and the noisy ambient would indicate that the tests should be made in a shielded enclosure. Unfortunately, all shielded enclosures introduce significant errors into the radiated measurements because of room reflections, room resonances, and antenna loading. To reduce the magnitude of these problems, the FCC has specified that measurements should be made at an open-field test site. Open-field test sites frequently have high ambient levels especially in the FM broadcast band. They may also have ground reflection variations as a function of soil moisture.

The FCC will permit the use of anechoic shielded enclosures which have reduced reflections, provided an error analysis is made to show correlation of interior RF levels with those of an open-field test site. The cost of an anechoic enclosure is its major drawback. For measurements other than for certification, the test site does not have to be in accordance with government regulations. There are also alternatives where an agency or private company will perform the tests for you at their facility for a nominal fee.

Many manufacturers are using shielded enclosures that they have constructed on site or purchased from one of the shielded enclosures manufacturers. The measurement requirement is that the RF ambient levels should be 6 dB or more below the specifications limits. This may require 20 dB worth of aluminum foil or 160 dB worth of electrical seals. Only a site survey can provide that answer. In any case, some margin of safety should be made, 6–10 dB, plus periodic check for reflection problems.

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25 Instrumentation

After the appropriate test site has been obtained, whether a room or a quiet open field, then the testing can begin. If the equipment to be tested is not floor standing, the test sample is placed on a non-conducting stand 80 cm high and at least 40 cm from the wall of the enclosure. Antennas are then set up so that radiated emission levels can be measured. The test sample should be loaded with full electrical and mechanical loads and operated in a manner that closely approximates normal operation. During operation of the equipment under test, the EMI measuring equipment is used to determine the amplitude of the radiated emission.

At NSC, we have a spectrum analyzer than can be attached to a Personal Computer that runs software to control experiments and report results. It automatically marks the computer display with FCC limits for quick comparison with the amplitude of the emissions signal. This setup is outside the shielded enclosure and can be used to determine if the equipment under test is failing any FCC requirements.

If the test sample fails, we can move inside the room and use near-field probes to help pinpoint the source of emissions. The spectrum analyzer samples the signal generated by the source at many different frequencies. The scale across the bottom of the screen is frequency and the scale along the side is signal amplitude in dBuV/m. Thus, we can quickly determine where the peak amplitude of the generated noise is located, read what level that is, and at what frequency it is being generated.

A little analysis and thought should then allow you to determine what signal could be the culprit. For example, if the noise problem is at 16 MHz and the system clock is 16 MHz, then the basic clock signal is causing the problem. If the noise problem is at even multiples of 16 MHz it could be caused by rise and fall times on the 16 MHz clock or overshoot and undershoot on that clock. In the case of the HPC, since it generates a clock output that is the system clock divided by 2 (CK2 = CKI/2), the noise frequency generated at the multiple of the 16 MHz signal could also be due to CK2 or any device that is clocked by that signal. Unfortunately for the investigator, everything else inside the part is clocked by CK2, which includes bus transitions and input sampling.

26 Cost

Basically, the risks of no EMI control will include the following:

- Vehicle/System Performance Degradation
- Degradation to outside world equipment
- Personal Hazards
- Ordinance Hazards
- Acceptance Delays

The sum which can mean anything from a minor system or equipment performance compromise to the total cancellation of a project.

The cost of EMI control will vary and include the following:

- Government procurement requirements
- Company proposal preparation
- EMI Control Plan
- Test Plan
- EMI Tests and Reports

A rough guideline that can be used might be:

1%–3% of $100 Million projects

3%–7% of $1 Million to $10 Million projects 7%–12% of small items

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27 SUMMARY

The design and construction of an electromagnetically compatible printed circuit board does not necessarily require a big change in current practices. On the contrary, the implementation of EMC principles during the design process can fit in with the ongoing design. When EMC is designed into the board, the requirements to shield circuitry, cables, and enclosures, as well as other costly eleventh hour surprises, will be drastically reduced or even eliminated. Without EMC in the design stage, production can be held up and the cost of the project increases.

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